



## **APPLICATION NOTE: AN102**

# **StreamStor PCI-816XF/XF2 FPDP Implementation Details**

Rev. E, November 30, 2003

## **Overview and Background**

To improve connectivity for its customers, Conduant Corporation has added FPDP interface connections on its StreamStor line of PCI recording products. While making every effort to conform to ANSI/VITA 17-1998 (the official FPDP standard, referred to as “the standard”), the StreamStor controller implementation is a superset of that described in the standard. This document elaborates on those differences and also the hardware used to implement the interface. It assumes that the reader is familiar with the contents of the standard and understands the function of the various integrated circuits.

## **Superset Features**

StreamStor implements most of the features specified in the standard while adding additional capabilities that have been driven by customer requirements. In addition to the FPDP/TM, FPDP/R, and FPDP/RM modes that are described in the standard, StreamStor also implements the following modes:

- FPDP/T mode – FPDP Transmit
- FPDP/RMCM mode – FPDP Receive Master Clock Master
- Bus operation up to 50MHz for 200Mbyte/s throughput

In FPDP/T mode, StreamStor drives the FPDP DATA, DVALID\* (Data Valid), DIR\* (direction), and SYNC\* (Sync Pulse) signals but uses the FPDP clock that is driven to the FPDP bus by some other source. In this mode, StreamStor does not provide any termination for signals other than DATA<sup>1</sup>. To use this mode properly, StreamStor should NOT be positioned at either end of the FPDP bus. Since the data source is not the clock source, note that the maximum useable frequency in this mode will decay more rapidly as the cumulative distance from the clock source to the data source to the data destination increases.

In FPDP/RMCM mode, StreamStor acts as a Receive Master, excepting that StreamStor also drives the FPDP clock signals on the FPDP bus. In addition, StreamStor terminates the clock signals (PSTROBE, PSTROBE\*, and STROB) as would a traditional FPDP/TM while terminating the remaining signals as would a FPDP/RM. To use this mode StreamStor should be physically positioned at an end of the FPDP bus. Since the data source is not the clock source, note that the maximum useable frequency in this mode will decay more rapidly as the cumulative distance from the clock source to the data source to the data destination increases.

## **Frame Data Modes**

StreamStor has implemented FPDP Single Frame Data mode both for recording and playback as described in the specification. Repeating Frame Data modes are not currently supported.

## **Not Supported**

StreamStor does not currently support FPDP Repeating Frame Data modes.

StreamStor does not use the PIO signals. It neither drives nor acts on the state of the PIO signals.

The StreamStor controller can be electronically upgraded, if required, to add Repeating Frame Mode and/or PIO signal support.

StreamStor does not currently support method 2 termination of PSTROBE/PSTROBE\*.

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<sup>1</sup> StreamStor always provides series termination on the DATA signals as described in Permission 6.4.1 of the ANSI specification.

## Components

While the standard refers to various parts by part number for different signals, there are actually several speed grades available for most of the specified parts. Because StreamStor is able to operate at rates faster than the maximum 40MHz specified in the standard, StreamStor utilizes the faster speed grade parts in each family of parts. This minimizes actual propagation, setup, and hold time requirements to their minimums though the standard may specify higher values. The actual chips used on StreamStor are:

Signal	Transmitter	Receiver
D<31:0>	IDT74FCT16952ETPA	IDT74FCT16952ETPA
STROB	IDT49FCT805BTPY	IDT49FCT805BTPY
DVALID*,SYNC*	IDT74FCT16952ETPA	IDT74FCT16952ETPA
PSTROBE,PSTROBE*	MC10ELT28D	MC10ELT28D
PIO1,PIO2	IDT74FCT16245ATPA	IDT74FCT16245ATPA
SUSPEND*,DIR*,NRDY*	74F3038D	74F3038D

**Table 1 - Components used in StreamStor FPDP implementation.**

Note that the STROB signal uses the IDT49FCT805 part instead of the IDT49FCT806. The 805 is simply the non-inverting version of the 806 and does not affect equivalency. Also note that DVALID\* and SYNC\* are specified by the standard to use a IDT74FCT16245 when driven by the transmitter while the actual StreamStor implementation uses the IDT74FCT16952. While one is a registered device and the other is not, the devices are comparable for meeting drive and timing requirements.

## Timing

All timing on StreamStor is referenced to the clocks on the FPDP bus. This applies regardless of whether StreamStor is driving the bus clocks or receiving them. When driving the bus clocks, StreamStor immediately receives the clocks that it just drove to the bus and performs its activity with respect to the received clock, not the transmitted clock. This implementation ensures consistent behavior regardless of the mode of operation and timing that is completely synchronous to that of other devices on the bus.

Actual timings measured on a short (4 inches) FPDP bus with one StreamStor FPDP/TM and one StreamStor FPDP/RM and 2ns sampling are shown below. Note that while STROB timing is shown for 40 and 50MHz, STROB is not recommended for use above 20MHz. At slower frequencies, the hold times will remain the same while the setup times will increase by the increase in the clock period. Measured times are as follows:

### 40MHz Clock:

Clock Duty cycle = 50%  
Tsu DVALID\* and DATA to STROB = 12 - 14ns  
Th STROB to DATA,DVALID\* = 10ns

Tsu DVALID\* and DATA to PSTROBE = 10 - 14ns  
Th PSTROBE to DATA,DVALID\* = 12ns

### 50MHz Clock:

Clock Duty cycle = 50%  
Tsu DVALID\* and DATA to STROB = 7 - 9ns  
Th STROB to DATA,DVALID\* = 10ns

Tsu DVALID\* and DATA to PSTROBE = 5 - 9ns  
Th PSTROBE to DATA,DVALID\* = 12ns

## **Crossbar Switches**

Many of the chips used on the FPDP interface are inherently bi-directional due to their tri-state or open-collector driver design. This greatly simplifies the ability to implement an FPDP interface that can be electronically switched under software control to the different modes supported by StreamStor. In addition, permission 6.4.1 of the standard allows for the series terminators on D<31:0> to be always installed regardless of the direction of transfer, thus eliminating the need to switch data terminators in or out based on the direction of transfer.

Some termination networks, however, are not symmetrical with respect to the direction of transfer. Furthermore, some drivers do not have tri-state or open-collector implementations. These termination networks and drivers are connected, as needed, to the appropriate FPDP signals using IDT74FST3125Q crossbar switches. When closed, these switches propagate signals with a delay of only 250 picoseconds and appear as a 5 ohm series resistor. When open, the two ports of the switch are isolated with high impedance.

With regard to the direction of transfer, the process of changing FPDP modes via the XLRSetFPDPMODE function in the StreamStor API performs the following changes in the electronics:

- Changes the direction of transfer of the appropriate tri-state and open-collector devices, thus producing a change in signal direction, and
- Connects the appropriate termination network to each signal based on the direction of transfer and the position on the FPDP bus.

Once a new mode has been set, each signal on the FPDP bus will be driven, received, and terminated as is defined in the FPDP specification for the direction of transfer for that signal, excepting that some of the termination networks and the differential clock signals will be connected through crossbar switches.

Note that StreamStor supports a superset of modes above what is described in the FPDP spec. While the additional modes do not match those described in the FPDP spec, the driver, receiver, and termination characteristics for each individual signal will be as defined in the spec for the corresponding direction of transfer and position on the FPDP bus.

## ***IMPORTANT: Non-inverted and Inverted FPDP Connectors***

Section 6.3.1, Figures 2 and 3, and Tables 2 and 3 of ANSI/VITA 17-1998 refer to inverted and non-inverted connector orientations. Tables 2 and 3 of the standard show how different cable conductors (and thus different signals) are connected to different connector pin numbers depending on which type of connector orientation is used. As shown in Figure 3 of the standard, a flat cable can connect two non-inverted, two inverted, or a mix of connectors together without rotating the cable. Referring to Figure 3 and Tables 2 and 3, notice that pin 1 of a non-inverted connector corresponds to cable conductor 1 while pin 80 of an inverted connector also corresponds to cable conductor 1. The different pinouts in the tables compensate for the different orientations. **IN A REAL WORLD ENVIRONMENT, IT IS ALSO POSSIBLE TO ENCOUNTER A NON-INVERTED CONNECTOR THAT HAS BEEN PHYSICALLY ROTATED. This could easily be mistaken for an inverted connector that could connect without cable rotation. For this situation, however, a cable connector must be rotated to establish the proper connection.**

**STREAMSTOR USES NON-INVERTED CONNECTORS.**

**Thus, it is important to know what kind of FPDP connector implementation is used on each board attached to the FPDP bus in order to properly connect the boards together. Failure to pay attention to this detail will, at the very least, prevent proper operation. In the worst scenario, THE INTERFACE ELECTRONICS ON ONE OR MORE BOARDS WILL BE DAMAGED.**

## ***Clocks and Clock Termination***

When acting in FPDP/TM or FPDP/RMCM modes, StreamStor drives both the PSTROBE differential pair clock and the STROB single-ended clock. In these modes, no driver termination is applied to STROB while method 1 driver termination is applied to PSTROBE and PSTROBE\*. The differential clock and method driver 1 termination are connected through two crossbar switches.

When acting in FPDP/T and FPDP/R modes, no clocks are driven by StreamStor and no termination is applied to any clock signals.

When acting in FPDP/RM mode, receiver termination is applied to STROB and method 1 receiver termination is applied to PSTROBE and PSTROBE\*. The differential termination is engaged using a single crossbar switch.

When acting in FPDP/T, FPDP/R, FPDP/RM and FPDP/RMCM modes, the clock to be used (PSTROBE/PSTROBE\* or STROB) for receiving data is selected by the user with the XLRSetFPDPMode API command. Refer to the “StreamStor Installation and Users Guide” for details about API commands.

Note that StreamStor is both a driver and receiver of clocks in FPDP/RMCM mode. This mode, when used in conjunction with FPDP/TM, can simplify the user implementation by using the StreamStor frequency synthesizer to generate FPDP bus clocks in both directions of transfer. Because StreamStor is the clock source in this mode, it must be positioned at one end of the FPDP bus and the user is responsible for providing clock termination at the other end of the FPDP bus. Note that the receiver termination on PSTROBE/PSTROBE\* provided by the user must be per method 1.

In the case of PSTROBE/PSTROBE\*, type 1 termination is engaged using crossbar switches when appropriate. When acting in FPDP/TM or FPDP/RMCM modes, StreamStor will drive the differential pair and terminate the pair with 330 ohm resistors to ground. When acting in FPDP/RM mode, a crossbar switch connects a 110 ohm resistor across the pair. In any other mode, no termination is applied to the pair.

Method 2 termination on PSTROBE/PSTROBE\* is not supported.

## ***Suspend\* Timing***

The standard indicates that a transmitter must deassert DVALID\* within 16 clocks of the assertion of SUSPEND\* by the receiver. For informational reference only, StreamStor actually deasserts DVALID\* in about 4 - 5 clocks after SUSPEND\* is asserted. Transfer will resume within about 3 clocks after SUSPEND\* is deasserted.

## ***Asynchronous Signals***

NRDY\* and SUSPEND\*, when received by StreamStor, are presumed to be asynchronous to the FPDP clocks. As such, StreamStor clocks these signals into a sequential series of two registers to synchronize them and minimize the possibility of metastable conditions. These signals are then acted on accordingly by the FPDP state machine.

## ***Summary***

Driven by customer requests, the StreamStor controller has evolved beyond the limitations of the original FPDP standard. StreamStor offers versatility through additional modes of operation and electronic reconfiguration, thus making it easy to reconfigure a system without moving cables or changing jumpers. StreamStor provides higher levels of performance with higher clock frequencies than are supported in the standard. These capabilities help make StreamStor the right component for your recording needs.

## ***Revision History***

- A. Initial Release.
- B. Added details of termination applied to PSTROBE/PSTROBE\*.
- C. Enhanced description of signal switching and termination.
- D. Addition of support for FPDP Single Frame Data Mode
- E. Addition of Conduant logo. Addition of section on Non-inverted and Inverted FPDP connectors.

## ***Rights and Trademarks***

StreamStor™ is a trademark of Conduant Corporation.