

APPLICATION NOTE: AN100

**CONNECTING TO STREAMSTOR CPCI-816 WITH A
PHYSICAL CHANNEL LINK CONNECTION AND A FPDP
PROTOCOL**

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Overview and Background

Conduant Corporation has implemented a connection to its CPCI-816 StreamStor controller that uses National Semiconductor's Channel Link (www.national.com) technology as a physical interface and FPDP (ANSI/VITA 17-1998, www.fdp.com) as the logical protocol.

The Conduant StreamStor CPCI-816 is a 6U CompactPCI recording/playback disk controller that enables long duration recording and playback of digital data at sustained minimum rates of up to 200Mbytes/sec. While the CPCI-816 can sustain these rates with direct card-to-card transfers over the PCI bus, the CPCI-816 also supports the direct connection of external equipment to dedicated I/O ports on a StreamStor controller daughter board. This allows for a much simpler and dedicated connection without all the encumbrances of moving data within the PC architecture.

Channel Link provides a method of compacting a wide, single-ended, synchronous parallel bus into a few high-speed LVDS signals plus a clock for transmission over cables, only to reconstruct the original parallel bus at the receiving end of the cable. This transmission medium allows FPDP to run at higher speeds over longer distances than would be possible using the ANSI standard interface. Because Channel Link is a unidirectional technology, a pair of Channel Link connections, one in each direction, was chosen to facilitate a full duplex connection that enables flow control and allows for electronic mode (FPDP transmitter or receiver) reconfiguration. Conduant uses the DS90CR483/484 transmitter/receiver chipset.

FPDP, as described in the ANSI standard, is a 32-bit parallel interface capable of transferring with clock rates up to 40MHz for data rates up to 160MBytes/s. In addition, a few signals (NRDY*, SUSPEND*) are provided for flow control (to prevent data overruns) and to provide delimiters (SYNC*), if desired, that identify boundaries between different packets of data. A data valid (DVALID*) signal is also provided to indicate on which rising edges of the FPDP clock data should be considered valid. FPDP is simple to implement and is ideal in applications where the main objective is to move data from one point to one-or-more destinations with little or no overhead.

CPCI-816 FPDP over Channel Link

Physical Interface

The Conduant CL-FPDP daughter board attaches to the CPCI-816. It provides a physical interface consisting of a pair of Channel Link connections, one in each direction, and a logical interface consisting of the FPDP signal set. The single-ended sides of the Channel Link chips look like LVTTTL representations of the 5V TTL FPDP signals defined in the ANSI/VITA specification. When designed from scratch, the designer can connect directly from the control logic to the two Channel Link chips, thus eliminating the many driver/receiver chips that would otherwise be required to implement the standard FPDP physical interface. Designers should, however, understand the LVTTTL input and output timing specifications for the Channel Link chip set prior to committing a design since the relative position of signals to clocks can change slightly from one end of the Channel Link connection to the other.

FPDP Operating Modes

The CL-FPDP board can be configured through API calls in the software to act either as a FPDP/TM (Transmit Master) or a FPDP/RM (Receive Master). In addition, API calls can set the FPDP/TM clock frequency from 33.33MHz (limited on the downside by the Channel Link chip set) to 50MHz. For implementations where the user intends to broadcast from a FPDP/TM to multiple receivers, Conduant also provides CL-FPDP-R daughter boards in a FPDP/R (receiver without termination) configuration.

Each Channel Link cable, one inbound and one outbound, carries a full set of signals that are required for operating in both FPDP/TM and FPDP/RM modes. This allows StreamStor to be electronically reconfigured to either mode. When operating as a FPDP/TM, StreamStor will set the signals normally associated with transmit mode to meaningful states on the transmit cable and it will ignore all but the SUSPEND* and NRDY* signals that are driven on the receive cable by the FPDP/RM card. Similarly, when operating as a FPDP/RM, StreamStor will set the SUSPEND* and NRDY* signals to meaningful states on its transmit cable and will monitor only the meaningful signals that is receiving from the FPDP/TM card.

FPDP Clocks

While a traditional FPDP physical interface provides for both a PECL differential clock (PSTROBE+/-) and a single ended TTL clock (STROB), the Channel Link interface includes a single LVDS clock that replaces both of these clocks.

When acting in the FPDP/TM mode, the FPDP clock generated on StreamStor can be programmed through the StreamStor API to frequencies from 33.33MHz (limited on the down side by the Channel Link chip set) through 50MHz for sustained minimum data rates up to 200MBytes/s. Data rates lower than 132MBytes/s (i.e. 33.33 MHz clock) will require that the user make use of the FPDP throttling controls (DVALID*, SUSPEND*, and NRDY*) to implement “wait states” on the FPDP bus.

FPDP Flow Control Note

In a traditional FPDP implementation, the SUSPEND* and NRDY* signals allow a receiver card to temporarily pause the the transmission of data by the transmitter so as to prevent a buffer overrun at the receiver. This is also the case with the StreamStor Channel Link implementation. A subtle implementation detail that is easy to overlook is that Channel Link chip set requires a clock signal for each direction of data transfer. While the clock for transmission of data and DVALID* by the transmitter is obvious, the fact that a clock must be provided to the Channel Link transmitter chip on the FPDP receiver card to transmit SUSPEND* and NRDY* to the transmitter card is less obvious. Any clock within the frequency range defined elsewhere in this document is acceptable regardless of the data clock since these signals will be treated as asynchronous inputs at the transmitter card. Failure to clock the flow control signals through the Channel Link in the return direction will defeat flow control and may even cause the transmitter card to read the received flow control signals as permanently in the paused state.

FPDP to Channel Link User Signal Mapping

The user interfaces on the Channel Link transmitters and receivers are 48 bits wide. Since FPDP does not require 48 connections, unused transmitter inputs should be driven LOW to eliminate any problems that could be introduced due to floating inputs. This also keeps the currently unused signals in a known state and allows for the addition of additional features, if needed.

Table 1 shows the mapping of FPDP signals to the Channel Link transmitter (DS90CR483) single-ended input pins. Table 2 shows the mapping of FPDP signals to the Channel Link receiver (DS90CR484) single-ended output pins. This mapping can be used by third parties to design Channel Link FPDP cards that are compatible with StreamStor. However, it is recommended that third parties contact Conduant Corporation prior to implementation to get any updates that may not be specified in this application note.

FPDP Signal Name	CR483 Signal Name	CR483 Pin #		FPDP Signal Name	CR483 Signal Name	CR483 Pin #		FPDP Signal Name	CR483 Signal Name	CR483 Pin #
D0	TxIN0	10		D16	TxIN16	92		DIR*	TxIN32	74
D1	TxIN1	9		D17	TxIN17	91		DVALID*	TxIN33	73
D2	TxIN2	8		D18	TxIN18	90		NRDY*	TxIN34	72
D3	TxIN3	7		D19	TxIN19	89		PIO1	TxIN35	71
D4	TxIN4	6		D20	TxIN20	88		PIO2	TxIN36	70
D5	TxIN5	5		D21	TxIN21	87		CLK	TxCLKIN	11
D6	TxIN6	4		D22	TxIN22	86		SUSPEND*	TxIN37	69
D7	TxIN7	3		D23	TxIN23	85		SYNC*	TxIN38	66
D8	TxIN8	2		D24	TxIN24	84		unused	TxIN39	65
D9	TxIN9	1		D25	TxIN25	81		unused	TxIN40	64
D10	TxIN10	100		D26	TxIN26	80		unused	TxIN41	63
D11	TxIN11	99		D27	TxIN27	79		unused	TxIN42	62
D12	TxIN12	96		D28	TxIN28	78		unused	TxIN43	61
D13	TxIN13	95		D29	TxIN29	77		unused	TxIN44	60
D14	TxIN14	94		D30	TxIN30	76		unused	TxIN45	59
D15	TxIN15	93		D31	TxIN31	75		unused	TxIN46	58
								unused	TxIN47	57

Table 1 - FPDP Signal to DS90CR483 Channel Link Transmitter Pin Map

FPDP Signal Name	CR484 Signal Name	CR484 Pin #		FPDP Signal Name	CR484 Signal Name	CR484 Pin #		FPDP Signal Name	CR484 Signal Name	CR484 Pin #
D0	RxOUT0	8		D16	RxOUT16	28		DIR*	RxOUT32	49
D1	RxOUT1	9		D17	RxOUT17	29		DVALID*	RxOUT33	50
D2	RxOUT2	10		D18	RxOUT18	30		NRDY*	RxOUT34	51
D3	RxOUT3	11		D19	RxOUT19	31		PIO1	RxOUT35	52
D4	RxOUT4	12		D20	RxOUT20	32		PIO2	RxOUT36	53
D5	RxOUT5	14		D21	RxOUT21	34		CLK	RxCLKOUT	42
D6	RxOUT6	15		D22	RxOUT22	36		SUSPEND*	RxOUT37	55
D7	RxOUT7	17		D23	RxOUT23	37		SYNC*	RxOUT38	57
D8	RxOUT8	18		D24	RxOUT24	38		unused	RxOUT39	58
D9	RxOUT9	19		D25	RxOUT25	39		unused	RxOUT40	59
D10	RxOUT10	20		D26	RxOUT26	40		unused	RxOUT41	60
D11	RxOUT11	21		D27	RxOUT27	41		unused	RxOUT42	61
D12	RxOUT12	22		D28	RxOUT28	43		unused	RxOUT43	62
D13	RxOUT13	24		D29	RxOUT29	46		unused	RxOUT44	64
D14	RxOUT14	26		D30	RxOUT30	47		unused	RxOUT45	65
D15	RxOUT15	27		D31	RxOUT31	48		unused	RxOUT46	67
								unused	RxOUT47	68

Table 2 - FPDP Signal to DS90CR484 Channel Link Receiver Pin Map

Channel Link LVDS Signal Mapping to Cable Connector

The 48 single-ended signals plus a clock are packed and mapped by the DS90CR483 to 8 differential signal pairs plus a differential clock pair. The CL-FPDP board has two 26-pin connectors (3M P/N 10226-55G3VC), one for transmitting the Channel Link signals and the other for receiving Channel Link signals. Table 3 shows the signal mapping from the DS90CR483 to the 26-pin transmitter connector and Table 4 shows the signal mapping from the DS90CR484 to the 26-pin receiver connector.

Connector Pin #	CR483 Signal Name	CR483 Pin #	Connector Pin #	CR483 Signal Name	CR483 Pin #	Connector Pin #	CR483 Signal Name	CR483 Pin #
1	inner shield	n/a	10	TxOUTM7	29	19	TxOUTP3	38
2	TxOUTM0	50	11	GND	n/a	20	TxOUTP4	36
3	TxOUTM1	47	12	GND	n/a	21	TxOUTP5	33
4	TxOUTM2	45	13	inner shield	n/a	22	TxOUTP6	31
5	TxCLKM	42	14	inner shield	n/a	23	TxOUTP7	28
6	TxOUTM3	39	15	TxOUTP0	49	24	GND	n/a
7	TxOUTM4	37	16	TxOUTP1	46	25	GND	n/a
8	TxOUTM5	34	17	TxOUTP2	44	26	inner shield	n/a
9	TxOUTM6	32	18	TxCLKP	41			

NOTE: The CL-FPDP boards connect the inner shield to digital GND.

Table 3 – Channel Link Signal Mapping from DS90CR483 to 26-pin connector

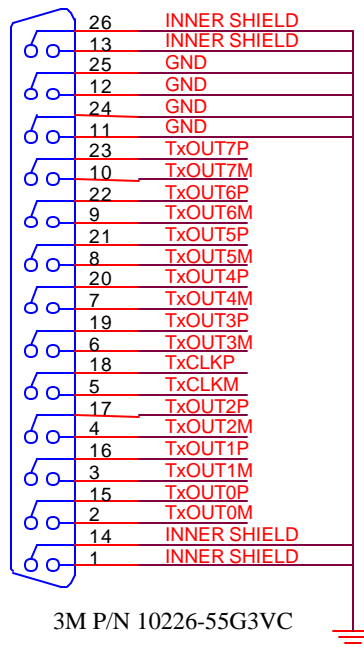


Figure 1 – Schematic for DS90CR483 connection to 26-pin transmitter connector

Connector Pin #	CR484 Signal Name	CR484 Pin #	Connector Pin #	CR484 Signal Name	CR484 Pin #	Connector Pin #	CR484 Signal Name	CR484 Pin #
1	inner shield	n/a	10	RxINM7	80	19	RxINP3	89
2	RxINM0	99	11	GND	n/a	20	RxINP4	86
3	RxINM1	97	12	GND	n/a	21	RxINP5	84
4	RxINM2	95	13	inner shield	n/a	22	RxINP6	82
5	RxCLKM	100	14	inner shield	n/a	23	RxINP7	79
6	RxINM3	90	15	RxINP0	98	24	GND	n/a
7	RxINM4	87	16	RxINP1	96	25	GND	n/a
8	RxINM5	85	17	RxINP2	94	26	inner shield	n/a
9	RxINM6	83	18	RxCLKP	91			

NOTE: The CL-FPDP boards connect the inner shield to digital GND.

Table 4 – Channel Link Signal Mapping from DS90CR484 to 26-pin receiver connector

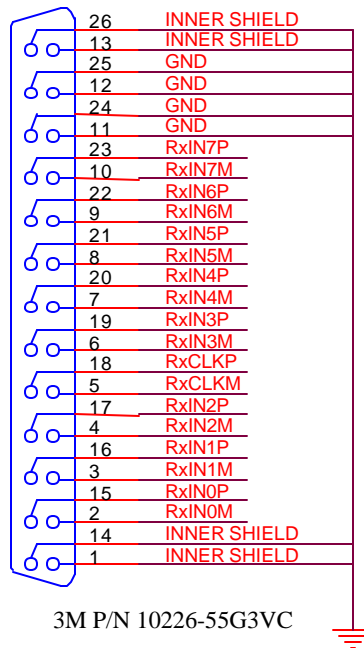


Figure 2 – Schematic for DS90CR484 connection to 26-pin connector

Cables

Channel Link is a technology based on high-frequency LVDS (Low Voltage Differential Signaling). The Channel Link interface specific to the DS90CR483/484 chip set consists of 8 differential pairs for data and one additional pair for the clock.

The pinouts on the transmitter and receiver Channel Link connectors on the CL-FPDP daughter board have the same orientation. For example, TxOUT0M is pin 2 on the transmitter connector while RxIN0M is pin 2 on the receiver connector. Thus, the signals would connect up correctly between transmitter and receiver connectors with the orientation shown above when using a “straight-thru” cable.

While there may be other suitable product cables available, 3M manufactures a series of standard product cables that are intended for the Camera Link (a Channel Link-based interface) industry standard interface. These cables are specifically designed to support the high-speed LVDS signals generated by Channel Link. The Camera Link cable, 3M family part number 14x26-SZLB-xxx-0LC (where ‘x’ is substituted with various option parameters), is available in different lengths from 1 to 10 meters. Note, however, that these cables axially rotate the signals 180 degrees from one end of the cable to the other (i.e. pin 2 at one end of the cable is connected to pin 25 at the other end of the cable, etc.). If one plans to use these cables to connect to StreamStor, they should consider designing their boards with their signals axially rotated from the connector pinouts shown in figures 1 and 2. Another possibility is to remove and rotate the metal header around the connector on one end of the Camera Link cable, thus making it a straight-thru cable. We have done this quite easily in the past but we cannot guarantee that 3M will not change their manufacturing process in the future making this solution difficult or impossible.

Multiple Target Operation

A traditional FPDP physical interface supports multiple receivers on a bus, any one of which can throttle the data transmission by asserting the open-collector SUSPEND* and NRDY* signals. This allows the implementation of an open-loop “broadcast” system. With a Channel Link connection, there can be multiple receivers (FPDP/R) so long as only the last one on the bus (FPDP/RM) provides termination. However, it is not possible with Channel Link to allow multiple receivers to drive these throttling signals back to the FPDP/TM. Only a single destination will be able to do that. The solution is to ensure that all the receivers have the bandwidth to receive data at clock rates of a minimum of 33.33 MHz (132 MBytes/s) or to use a “broadcast” configuration only in applications where the receivers are allowed to discard data when they cannot keep up.

Termination and board layout

Channel Link is a high-frequency technology that requires specific termination and board layout implementations. Refer to the National Semiconductor website (www.national.com) for data sheets on the DS90CR483/484 chipset and also various application notes regarding Channel Link, including one for board layout recommendations.

Summary

The simplicity of the FPDP protocol and the completeness of the Channel Link chip set facilitate an easy and cost effective hardware implementation for high-speed, medium distance point-to-point data transfer. This solution significantly extends the distances that would otherwise be possible with the ANSI standard physical interface. All the components, including cables, are readily available to quickly implement such a connection to a StreamStor CPCI-816/CL-FPDP controller.

Revisions

Rev C: - Added section "FPDP Flow Control Note". Added Conduant logo.

Rev D: - Changed Conduant logo.

Rights and Trademarks

StreamStor™ is a trademark of Conduant Corporation.

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