APPLICATION NOTE: AN103

StreamStor FPDP-II Implementation Details

Rev. D, February 14, 2007

IMPORTANT NOTE: For FPDP functional and connector information relating to PCI-816XF/XF2, please refer to Conduant Application Note AN102. AN103 is specific to StreamStor Amazon FPDP Mezzanine boards.

Overview and Background

StreamStor Amazon is a high speed recording and playback system that makes use of interchangeable interface boards. One such board has a pair of FPDP-II interfaces, each of which is able to sustain recording or playback rates up to 400 Mbytes/s.

ANSI/VITA 17-1998 (the official FPDP standard, referred to as "the standard"), defines the original implementation which provides for a peak transfer rate of 160MB/s. However, many companies, including Conduant, offer a superset level of performance by running the FPDP clock up to 50 MHz for a transfer rate of up to 200MB/s. The FPDP-II functionality that proposed 400MB/s transfer rates grew out of the fact that many companies operated their busses with a 50MHz clock. By keeping the same clock speed but changing the data bus timing to operate in DDR (Double Data Rate) mode, the sustained data rate doubled from 200MB/s to 400MB/s. While a draft for this standard had been previously created and was posted on www.fpdp.com, it never evolved into an official standard. Nonetheless, several companies now offer FPDP-II products that are based on that earlier draft.

The StreamStor FPDP-II interface is backwards compatible with the original FPDP standard and its 200MB/s superset in addition to offering the 400MB/s DDR implementation. In addition, StreamStor supports some additional capabilities which customers may find useful.

While relying on the standard for reference, this document specifically describes the StreamStor FPDP-II implementation. This information is useful for those who plan to attach third party FPDP boards or who plan to design FPDP-II interface boards to attach to StreamStor products. It is assumed that the reader is familiar with the contents of the standard and understands the function of the various integrated circuits.

Superset Features

In addition to the 50MHz clock speed discussed, StreamStor implements some superset features that are not part of the standard. These have evolved due to customer requests to add flexibility. In addition to the FPDP/TM, FPDP/R, and FPDP/RM modes that are described in the standard, StreamStor also implements the following modes:

- FPDP/T mode – FPDP Transmit
- FPDP/RMCM mode – FPDP Receive Master Clock Master
- Event Capture – Inquire with Conduant Sales as to the availability of this feature on the FPDP-II daughterboard.

In FPDP/T mode, StreamStor drives the FPDP DATA, DVALID* (Data Valid), and DIR* (direction) signals but uses the FPDP clock that is driven to the FPDP bus by some other source. In this mode, StreamStor does not provide any termination for signals other than DATA[1]. To use this mode properly, StreamStor should NOT be positioned at either end of the FPDP bus. Since the data source is not the clock source, note that the maximum useable frequency in this mode will decay more rapidly as the cumulative distance from the clock source to the data source to the data destination increases.

In FPDP/RMCM mode, StreamStor acts as a Receive Master, except that StreamStor also drives the FPDP clock signals on the FPDP bus. In addition, StreamStor terminates the clock signals (PSTROBE, PSTROBE*, and STROB) as would a traditional FPDP/TM while terminating the remaining signals as would a FPDP/RM. To use this mode StreamStor should be physically positioned at an end of the FPDP bus. Since the data source is not the clock source, note that the maximum useable frequency in this mode will decay more rapidly as the cumulative distance from the clock source to the data source to the data destination increases. Since FPDP uses single ended signals and an unshielded cable, the analog characteristics of transmitted signals and optimal bus timing also affects maximum cable length, especially at higher clock rates.

[1] StreamStor always provides series termination on the DATA signals as described in Permission 6.4.1 of the ANSI specification.

Event Capture saves the exact offsets from the beginning of a recording of one or more events that occur while recording. The events are identified by the data source with rising and/or falling transitions on any or all of the SYNC*, PIO1, and PIO2. At the completion of the recording, the user can download the event list to use when analyzing the data. Conceptually, one can think of this as a continuously running, gap free logic analyzer with a multiple, simple trigger system.

Frame Data Modes

StreamStor Amazon implements the unframed data mode of FPDP specification. For FPDP Single Frame Data mode contact Conduant Corporation. Repeating Frame Data modes are not currently supported.

Not Supported

StreamStor Amazon does not currently support FPDP Single Frame or Repeating Frame Data modes.

StreamStor does not use the PIO signals. It neither drives nor acts on the state of the PIO signals.

The StreamStor controller can be electronically upgraded, if required, to add Single Frame mode, Repeating Frame Mode and/or PIO signal support.

StreamStor does not currently support method 2 termination of PSTROBE/PSTROBE*.

FPDP bus signaling

FPDP connections are consistent with the FPDP standard with the exception of the ground on pin 15 of the non-inverted connection (pin 17-B or 66 on an inverted connector) which is reserved for FPDP-II mode control. FPDP-II mode is active high with a weak pull up to allow board sensing of a bus. If the line is low, one or more boards that are only capable of FPDP mode 1 are present, and all boards on the bus run in FPDP mode 1. If the line is sensed high, the bus runs in FPDP mode 2. StreamStor Amazon has a programmable driver to disable the FPDP-II mode on the bus as needed using an option to XLRSetDBMode.

The FPDP standard refers to various parts by part number for different signals. In order to implement double data rate, similar drivers were used. The TI LVTH family is used for TTL signals. The 74F3038D is retained for hardware data flow control signals SUSPEND, DIR, and NRDY. The LVTH parts used for data accept FPDP bus signals at 5 Volt TTL levels and drive out with signal levels compatible with 5V TTL. The drivers are powered from 3.3 Volt, so steady state signals will remain at 3.3 Volt levels. This is consistent with other instrumentation products and helps address the primary sources of signal integrity issues inherent in a wide bus of single ended data.

Because StreamStor is able to operate at rates faster than the maximum 40MHz specified in the standard, StreamStor utilizes the higher performance parts for clock drivers and receivers. PECL clocks are driven referenced to 5V, and received with a 5V referenced receiver DC coupled. Since there is no phase lock loop on the received clock signals, TTL or PECL, the StreamStor receiver is static. Flow control should be implemented with data valid, but StreamStor tolerates a temporarily stopped clock.

When designing to be interoperable with StreamStor FPDP II equipment, two important points are digital timing and analog signal integrity. The setup and hold time requirements must first be accomplished including clock rise time, skew (clock to data and channel to channel), and other clock characteristics. The analog signal issues resulting from using single ended bused signals over long cable include simultaneously switching noise and reflection. A solid ground reference and good slew rates with minimal ringing maximizes the clock rate that can be used on any given length of cable.

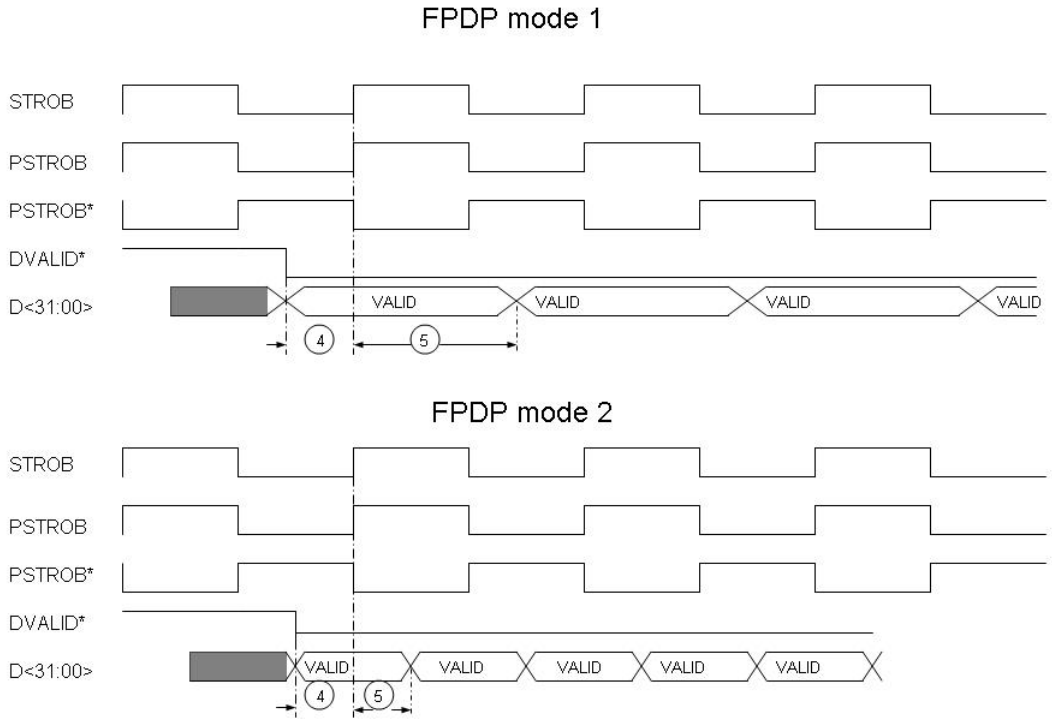
Timing

All timing on StreamStor is referenced to the clocks on the FPDP bus. Base timing starts with compatibility to the FPDP specification for mode 1 operation. When in FPDP mode 2, timing requirements meet the industry informal standard which is specified below.

Table 1 – FPDP-II timing specifications for TTL STROB and PECL PSTROB

	Parameter	At transmitter end of cable	At receiver end of cable
1	STROBE period	20 ns min.	20 ns min.
2	STROBE low	9.0 ns min.	9.0 ns min.
3	STROBE high	9.0 ns min.	9.0 ns min.
4	DATA, DVALID*, & SYNC* Setup to clock edge	5.5 ns min.	4.5 ns min.
5	DATA, DVALID*, & SYNC* Hold from clock edge	1.5 ns min.	0.5 ns min.
6	SUSPEND* active to DVALID* negated	16 STROBE period max.	16 STROBE period max.
7	SUSPEND* negated to DVALID* re-asserted	1 STROBE min.	1 STROBE min.

Note: When in FPDP mode 1, data hold time reverts to the original FPDP timing specification of 12 nS at the transmitter end of the cable. For faster frequencies than 40 MHz, in FPDP 1 mode, hold time is maximized.



When driving the bus clocks, StreamStor uses three independent taps from a phase lock loop (PLL) to drive output data, the TTL clock, and the PECL clock. Each clock output is individually and dynamically phase aligned to meet FPDP timing on the bus when a frequency is set. When receiving the bus clock, StreamStor uses it directly with only an input buffer, no PLL.

For example performance, actual timing was measured on a 12 inches unshielded cabled and a 1 meter shielded cabled FPDP bus with one StreamStor FPDP/TM and one StreamStor FPDP/RM. Measurements were taken with a 1 GS/s digital sampling Oscilloscope and are shown below. For FPDP mode 2 at slower frequencies, the hold times will remain the same while the setup times will increase by the increase in the clock period. For FPDP mode 1, data transitions with a fixed hold time from the falling clock edge. So, for FPDP mode 1, both setup and hold times increase as clock frequency reduces.

Example measured times are as follows:
PLL settings in firmware at version 12.16, FPDP2 load version 1.01, 11/30/2005.
Amazon #1507 & FPDP2 #2522 driven to Amazon #1519 & FPDP2 #2514.

	12 inch cable Tsu	12 inch cable Th	1 meter calbe Tsu	1 meter calbe Th
50 MHz Rising edge	6.5 nS	3.0 nS	5.0 nS	4.0 nS
50 MHz Falling edge	7.0 nS	3.0 nS	6.0 nS	4.0 nS
32 MHz Rising edge	>12 nS	3.0 nS	11.5 nS	3.3 nS
32 MHz Falling edge	>12 nS	3.1 nS	>12 nS	4.0 nS
10 MHz Rising edge	>15 nS	3.1 nS	>15 nS	2.6 nS
10 MHz Falling edge	>15 nS	3.3 nS	>15 nS	3.1 nS

For FPDP mode 1, data transitions one hold-time after a falling clock edge. So, setup time is one clock half period minus the FPDP2 data hold time, and hold time is one clock half period plus the FPDP2 data hold time.

Cable length, cable routing, and Conduant firmware releases level will effect actual bus timing observed.

Crossbar Switches

Many of the chips used on the FPDP interface are inherently bi-directional due to their tri-state or open-collector driver design. This greatly simplifies the ability to implement an FPDP interface that can be electronically switched under software control to the different modes supported by StreamStor. In addition, permission 6.4.1 of the standard allows for the series terminators on D<31:0> to be always installed regardless of the direction of transfer, thus eliminating the need to switch data terminators in or out based on the direction of transfer.

Some termination networks, however, are not symmetrical with respect to the direction of transfer. Furthermore, some drivers do not have tri-state or open-collector implementations. These termination networks and drivers are connected, as needed, to the appropriate FPDP signals using FET crossbar switches. When closed, these switches propagate signals with a delay of only 250 picoseconds and appear as a 4 ohm series resistor. When open, the two ports of the switch are isolated with high impedance.

With regard to the direction of transfer, the process of changing FPDP modes via the StreamStor API performs the following changes in the electronics:

- Changes the direction of transfer of the appropriate tri-state and open-collector devices, thus producing a change in signal direction, and
- Connects the appropriate termination network to each signal based on the direction of transfer and the position on the FPDP bus.

Once a new mode has been set, each signal on the FPDP bus will be driven, received, and terminated as is defined in the FPDP specification for the direction of transfer for that signal, excepting that some of the termination networks and the differential clock signals will be connected through crossbar switches.

Note that StreamStor supports a superset of modes above what is described in the FPDP spec. While the additional modes do not match those described in the FPDP spec, the driver, receiver, and termination characteristics for each individual signal will be as defined in the spec for the corresponding direction of transfer and position on the FPDP bus.

IMPORTANT: Non-inverted and Inverted FPDP Connectors

Section 6.3.1, Figures 2 and 3, and Tables 2 and 3 of ANSI/VITA 17-1998 refer to inverted and non-inverted connector orientations. Tables 2 and 3 of the standard show how different cable conductors (and thus different signals) are connected to different connector pin numbers depending on which type of connector orientation is used. As shown in Figure 3 of the standard, a flat cable can connect two non-inverted, two inverted, or a mix of connectors together without rotating the cable. Referring to Figure 3 and Tables 2 and 3, notice that pin 1 of a non-inverted connector corresponds to cable conductor 1 while pin 80 of an inverted connector also corresponds to cable conductor 1. The different pinouts in the tables compensate for the different orientations. IN A REAL WORLD ENVIRONMENT, IT IS ALSO POSSIBLE TO ENCOUNTER A NON-INVERTED CONNECTOR THAT HAS BEEN PHYSICALLY ROTATED. This could easily be mistaken for an inverted connector that could connect without cable rotation. For this situation, however, a cable connector must be rotated to establish the proper connection.

STREAMSTOR PCI-816XF2 USES NON-INVERTED FPDP CONNECTORS.
STREAMSTOR Amazon USES INVERTED FPDP CONNECTORS.

Thus, it is important to know what kind of FPDP connector implementation is used on each board attached to the FPDP bus in order to properly connect the boards together. Failure to be pay attention to this detail will, at the very least, prevent proper operation. In the worst scenario, THE INTERFACE ELECTRONICS ON ONE OR MORE BOARDS WILL BE DAMAGED.

Connectors used for Conduant FPDP port connections are consistent with the FPDP specification rule 6.3.1; 3M part number P50E-080P1-SR1-TG. Cabling can be bought directly from Conduant or assembled with 3M flat ribbon cable: 80 conductor 30 AWG, .025 spacing #3756/80. The mating connector used for cables is 3M P25E-080S-TG socket. And, an appropriate cable crimping tool is required to make cables.

Clocks and Clock Termination

When acting in FPDP/TM or FPDP/RMCM modes, StreamStor drives both the PSTROBE differential pair PECL clock and the STROB single-ended TTL clock. In these modes, no driver termination is applied to STROB while method 1 driver termination is applied to PSTROBE and PSTROBE*. The differential clock and method driver 1 termination are connected through two crossbar switches.

When acting in FPDP/T and FPDP/R modes, no clocks are driven by StreamStor and no termination is applied to any clock signals.

When acting in FPDP/RM mode, receiver termination is applied to STROB and method 1 receiver termination is applied to PSTROBE and PSTROBE*. The differential termination is engaged using a single crossbar switch.

When acting in FPDP/T, FPDP/R, FPDP/RM and FPDP/RMCM modes, the clock to be used (PSTROBE/PSTROBE* or STROB) for receiving data is selected by the user with an API command. Refer to the "StreamStor Installation and Users Guide" for details about API commands.

Note that StreamStor is both a driver and receiver of clocks in FPDP/RMCM mode. This mode, when used in conjunction with FPDP/TM, can simplify the user implementation by using the StreamStor frequency synthesizer to generate FPDP bus clocks in both directions of transfer. Because StreamStor is the clock source in this mode, it must be positioned at one end of the FPDP bus and the user is responsible for providing clock termination at the other end of the FPDP bus. Note that the receiver termination on PSTROBE/PSTROBE* provided by the user must be per method 1.

In the case of PSTROBE/PSTROBE*, type 1 termination is engaged using crossbar switches when appropriate. When acting in FPDP/TM or FPDP/RMCM modes, StreamStor will drive the differential pair and terminate the pair with 330 ohm resistors to ground. When acting in FPDP/RM mode, a crossbar switch connects a 110 ohm resistor across the pair. In any other mode, no termination is applied to the pair.

Method 2 termination on PSTROBE/PSTROBE* is not supported.

Suspend Timing*

The standard indicates that a transmitter must deassert DVALID* within 16 clocks of the assertion of SUSPEND* by the receiver. For informational reference only, StreamStor Amazon actually de-asserts DVALID* about 6 - 9 clocks after SUSPEND* is asserted. Transfer will resume within about 3 clocks after SUSPEND* is deasserted.

Asynchronous Signals

NRDY* and SUSPEND*, when received by StreamStor, are presumed to be asynchronous to the FPDP clocks. As such, StreamStor clocks these signals into a sequential series of two registers to synchronize them and minimize the possibility of metastable conditions. These signals are then acted on accordingly by the FPDP state machine.

Summary

Driven by customer requests, the StreamStor controller has evolved beyond the limitations of the original FPDP standard. StreamStor offers versatility through additional modes of operation and electronic reconfiguration, thus making it easy to reconfigure a system without moving cables or changing jumpers. StreamStor provides higher levels of performance with higher clock frequencies than are supported in the standard. These capabilities help make StreamStor the right component for your recording needs.

Revision History

A. Initial Release.
B. 11/2005 FPDP2 timing added from FPDP2 Draft specification. Additional descriptive text.
C. 6/2006 FPDP2 Lab characterization for cable lengths added.
D. 2/14/2007 - Added notation on the cover sheet that refers the reader to AN102 for information related to PCI-816XF/XF2 connector and functional information.

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